CLAIMS

1. A method for calculating pulse code modulated samples, said method comprising:

accessing an IMDCT sample from a previous set of IMDCT samples;

accessing an IMDCT sample from a present set of IMDCT samples;

calculating a first pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples; and

calculating a second pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples.

2. The method of claim 1, wherein calculating the second pulse code modulated sample comprises inverting the accessed IMDCT sample from the present set of IMDCT samples.

3. The method of claim 1, further comprising:

accessing a first inverse window coefficient; and

accessing a second inverse window coefficient.

4. The method of claim 3, wherein calculating the first pulse code modulated sample further comprises:

multiplying the accessed IMDCT sample from the previous set of IMDCT samples with the first inverse window coefficient; and

multiplying the accessed IMDCT sample from the present set of IMDCT samples with the second inverse window coefficient.

5. The method of claim 4, wherein calculating the second pulse code modulated samples further comprises:

accessing a third inverse window coefficient; and

accessing a fourth inverse window coefficient.

6. The method of claim 5, further comprising:

multiplying the accessed IMDCT sample from the previous set of IMDCT samples with a third inverse window coefficient; and

multiplying the accessed IMDCT sample from the present set of IMDCT samples with a fourth inverse window coefficient.

7. A system for calculating pulse code modulated samples, said method comprising:

a first address register for accessing an IMDCT sample from a previous set of IMDCT samples;

a second address register for accessing an IMDCT sample from a present set of IMDCT samples; and

an arithmetic logic unit for calculating a first pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples and calculating a second pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples.

8. The system of claim 7, wherein the arithmetic logic unit calculates the second PCM sample by inverting the accessed IMDCT sample from the present set of IMDCT samples.

9. The system of claim 7, further comprising:

a first memory for storing a portion of the previous set of IMDCT samples, the portion of the previous set of IMDCT samples comprising a last half of the previous set of IMDCT samples; and

a second memory for storing a portion of the present set of IMDCT samples, the portion of the present set of IMDCT samples comprising a first half of the present set of IMDCT samples.

10. The system of claim 9, further comprising:

a third memory for storing a plurality of inverse window coefficients.

11. The system of claim 10, further comprising:

a third address register for accessing a first one of the inverse window samples;

a fourth address register for accessing a second one of the inverse window samples;

a fifth address register for accessing a third one of the inverse window samples; and

a sixth address register for accessing a fourth one of the inverse window samples;

12. The system of claim 11, wherein the arithmetic logic unit multiplies the accessed IMDCT sample from the previous set of IMDCT samples with the first inverse window coefficient and multiplies the accessed IMDCT sample from the present set of IMDCT samples with the second inverse window coefficient.

13. The system of claim 12, wherein the arithmetic logic unit multiplies the accessed IMDCT sample from the previous set of IMDCT samples with the third inverse window coefficient and multiplies the accessed IMDCT sample from the present set of IMDCT samples with the fourth inverse window coefficient.

14. The system of claim 7, further comprising:

a fourth memory for storing the first pulse code modulated sample and the second pulse code modulated sample.

15. A circuit for calculating PCM samples, said circuit comprising:

a processor for executing a plurality of executable instructions;

an instruction memory for storing the plurality of executable instructions, wherein execution of the executable instructions causes:

accessing an IMDCT sample from a previous set of IMDCT samples from a first memory;

accessing an IMDCT sample from a present set of IMDCT samples from a second memory;

calculating a first pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples; and

calculating a second pulse code modulated sample from the accessed IMDCT sample from the previous set of IMDCT samples and the accessed IMDCT sample from the present set of IMDCT samples.

16. The circuit of claim 15, wherein the processor further comprises:

a first address register for referencing a memory location in the first memory, the memory location in the first memory storing the IMDCT sample from the previous set of IMDCT samples; and

a second address register for referencing a memory location in the second memory, the memory location

in the second memory storing the IMDCT samples from the present set of IMDCT samples.

17. The circuit of claim 16, wherein execution of the plurality of instructions further causes:

incrementing the first address register; and

incrementing the second address register.

18. The circuit of claim 17, wherein execution of the plurality of instructions further causes:

storing the first pulse code modulated sample in a memory location in a third memory; and

storing the second pulse code modulated sample in another memory location in the third memory.

19. The circuit of claim 18, wherein the processor further comprises:

a third address register for referencing the memory location in the third memory; and

a fourth address register for referencing the memory location in the fourth memory.

20. The circuit of claim 19, wherein execution of the plurality of instructions further causes:

incrementing the third address register; and

decrementing the fourth address register.